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Date: 09/21/2002

Time: 11:12

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	IS&R	4441	((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:02			0
2	BRS	4252	(((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and @ad<=20011115	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:02			0
3	BRS	58	((((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and @ad<=20011115) and (insulation with (dop$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:12			0
4	BRS	1818	((((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and @ad<=20011115) and ((insulation passivation insulating dielectric) with (etch$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:14			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
5	BRS	461	(((((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and @ad<=20011115) and ((insulation passivation insulating dielectric) with (etch$3))) and uniform	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:14			0
6	BRS	267	(((((((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and @ad<=20011115) and ((insulation passivation insulating dielectric) with (etch$3))) and uniform) and (dope doped doping impurity)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:26			0
7	BRS	16	(((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and (footing)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:28			0
8	BRS	0	bottom with dielectric with overetching with prevention	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 08:29			0
9	BRS	0	bottom with dielectric with (overetching footing) with prevention	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 08:29			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
10	BRS	29171	bottom with (insulating passivating) dielectric with (overetching footing) with (reduction minimization prevention)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:30			0
11	BRS	3281	(bottom with (insulating passivating) dielectric with (overetching footing) with (reduction minimization prevention)) and (((438/$) (216/$)).ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:31			0
12	BRS	251	((bottom with (insulating passivating) dielectric with (overetching footing) with (reduction minimization prevention)) and (((438/$) (216/$)).ccls.)) and ((control$5) with (doping doped dope impurity))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:33			0
13	BRS	239	(((bottom with (insulating passivating) dielectric with (overetching footing) with (reduction minimization prevention)) and (((438/$) (216/$)).ccls.)) and ((control$5) with (doping doped dope impurity))) and @ad<=20011115	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:37			0
14	BRS	400	(((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and (damascene hole via trench) and ((vertical with sidewall) (tappered) (sloped ramp))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:38			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
15	BRS	121	((((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and (damascene hole via trench) and ((vertical with sidewall) (tappered) (sloped ramp))) and ((dope doping dopant impurity) and (control controlled manipulation))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:39			0
16	BRS	119	(((((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and (damascene hole via trench) and ((vertical with sidewall) (tappered) (sloped ramp))) and ((dope doping dopant impurity) and (control controlled manipulation))) and @ad<=20011115	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 08:40			0
17	BRS	9	("3767492" | "4925805" | "5350484" | "5358908" | "5436174" | "5449630" | "5641380" | "5662768" | "5872045").PN.	USPAT	2002/09/19 09:08			0
18	BRS	8	3767492.URPN.	USPAT	2002/09/19 09:09			0
19	BRS	8	(((438/623) or (438/640) or (438/673) or (438/713) or (438/723) or (438/725) or (438/780) or (438/781) or (438/783) or (438/784) or (438/787) or (438/788) or (438/789) or (438/790) or (438/919) or (438/924)).CCLS.) and dopant with precursor with gas	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 09:10			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
20	BRS	167	dopant with precursor with gas	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 09:16			0
21	BRS	2518	(438/624).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 09:17			0
22	BRS	4	((438/624).ccls.) and footing	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 09:18			0
23	BRS	2945	dopant and precursor and gas	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 09:18			0
24	BRS	92847	(depositing forming) and (silicon adj (dioxide oxide))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 09:24			0
25	BRS	231	((depositing forming) and (silicon adj (dioxide oxide))) and (dopant with precursor) and gas	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 09:25			0
26	BRS	2891	((depositing forming) and (silicon adj (dioxide oxide))) and (adjust$3) and precursor and gas	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 09:26			0
27	BRS	471	(((depositing forming) and (silicon adj (dioxide oxide))) and (adjust$3) and precursor and gas) and dopant	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 09:27			0
28	BRS	450	(((((depositing forming) and (silicon adj (dioxide oxide))) and (adjust$3) and precursor and gas) and dopant) and @ad<=20011115	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 09:27			0
29	BRS	329	((((((depositing forming) and (silicon adj (dioxide oxide))) and (adjust$3) and precursor and gas) and dopant) and @ad<=20011115) and etch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 09:35			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
30	BRS	58	(((((((depositing forming) and (silicon adj (dioxide oxide))) and (adjust$3) and precursor and gas) and dopant) and @ad<=20011115) and etch$3) and (("phsub.3") ("sif.sub.4") ("b.sub.2h.sub.6"))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 09:41			0
31	BRS	40	(((((((depositing forming) and (silicon adj (dioxide oxide))) and (adjust$3) and precursor and gas) and dopant) and @ad<=20011115) and etch$3) and (("phsub.3") ("sif.sub.4") ("b.sub.2h.sub.6"))) and (((438/$) (257/$) (427/$) (216/$) (361/$)).ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 09:43			0
32	IS&R	2	("4795682").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 10:10			0
33	BRS	106	("NOVELLUS SYSTEMS, INC.").as.	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 10:19			0
34	BRS	724	((depositing forming) and (silicon adj (dioxide oxide))) and (defined with dopant)	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 10:29			0
35	BRS	56	(((depositing forming) and (silicon adj (dioxide oxide))) and (defined with dopant)) and (("ph.sub.3") ("sif.sub.4") ("b.sub.2h.sub.6"))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/19 10:43			0
36	IS&R	12	(("4698128") or ("5770469") or ("6051870") or ("6054206") or ("6165694") or ("6218284")).PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/19 10:45			0
37	BRS	4	("4732658" | "5157002" | "5817572" | "5908509").PN.	USPAT	2002/09/19 10:53			0
38	BRS	10	("4872947" | "4987102" | "5354611" | "5360646" | "5362526" | "5426076" | "5470802" | "5569058" | "5686031" | "5840631").PN.	USPAT	2002/09/19 10:53			0
39	BRS	32	4698128.URPN.	USPAT	2002/09/19 10:54			0

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40	BRS	7	("4217375" | "4972251" | "5104482" | "5231046" | "5268333" | "5278103" | "5286681").PN.	USPAT	2002/09/19 10:56			0
41	BRS	6	5770469.URPN.	USPAT	2002/09/19 10:57			0
42	BRS	4	6100202.URPN.	USPAT	2002/09/19 10:57			0
43	BRS	9	("4892753" | "5104482" | "5643828" | "5650041" | "5766992" | "5770469" | "5880019" | "5935340" | "5942446").PN.	USPAT	2002/09/19 10:58			0
44	BRS	951	(etch$3) with ((dope doped) with ((silicate adj glass) (silicon adj oxide)))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/20 07:39			0
45	BRS	561	((etch$3) with ((dope doped) with ((silicate adj glass) (silicon adj oxide)))) and (via hole	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/09/20 07:42			0
46	BRS	46	(((etch$3) with ((dope doped) with ((silicate adj glass) (silicon adj oxide)))) and (via hole damascene)) and (voids foot footing)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/20 07:42			0
47	BRS	3	("5879574" | "5976900" | "6218268").PN.	USPAT	2002/09/20 07:51			0

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Document Listing

D cument	Image pages	Text pages	Error pages
US 6426015 B1	0	5	0
Total	0	5	0

US-PAT-NO: **6426015**

DOCUMENT-IDENTIFIER: US 6426015 B1

TITLE: Method of reducing undesired etching of insulation due to elevated boron concentrations

-------- KWIC -------

Among the steps to which a silicon wafer is subjected in the course of processing into devices, such as high density DRAMs, is the step of applying to the devices a layer or layers of high temperature insulation. Typically, a thin glass-like layer containing silicon and other elements is used as the insulation. In the case of high density DRAMS, for example, the spaces separating one memory cell from another on the chip can be as narrow as a small
fraction of a micron in DRAMs now in production. The depth perpendicular to the face of the chip of such narrow spaces can be great enough that it becomes difficult to fully fill them with insulation free of **voids**.

A conventional way of applying insulation to semiconductor devices is to deposit silicon dioxide (SiO.sub.2) using chemical vapor deposition (CVD) onto the devices within a reaction chamber containing a gaseous mixture of tetraethylorthosilicate (TEOS) and ozone. As the film grows over the topographical surface, having spaces or gaps between elements of devices, the film thus fills the gaps. However, due to the nature of the reaction mechanism, the top surfaces of these gaps tend to receive more incoming reactant and thus higher growth rates, compared to the bottom portions. Therefore, **voids** tend to develop during the CVD process because of the greater depth-to-width ratio of the spaces in high-density semiconductor devices (e.g. gigabit DRAMS). To eliminate this difficulty TEOS is mixed in suitable proportion with triethylborate (TEB) and triethylphosphate (TEPO), as is well known in the art. The **voids** in insulation previously encountered are eliminated by the more "flowable" mixture of silicon, phosphorus and boron. But such an insulating layer in a thin zone where it touches or interfaces with bare surfaces of semiconductor elements (e.g., memory cells) of a device or with a dielectric layer, contains a much higher concentration of boron than contained elsewhere in the insulation. Thereafter when portions of insulation are selectively etched away using buffered hydrofluoric acid (BHP), as conventionally used in the art, the acid too aggressively attacks the

boron-rich zones of the insulation at the interface surfaces. This condition results in undesirable under cutting (or excessive etching away) of these boron-rich zones. This in turn exposes or lays bare conductive portions of elements of the device. When metal conductors are subsequently applied to the etched devices in a metalizing step, electrical short-circuits can occur. This clearly is an unacceptable condition.

Before applying insulation to the surfaces of semiconductors within a reaction chamber, it has been customary prior to the present invention to clean the chamber of residues of chemicals left over from a previous processing step. Then a semiconductor wafer is placed in the chamber and insulation is formed via CVD reaction of tetraethylorthosilicate (TEOS), triethylborate (TEB), triethylphosphate (TEPO) and ozone, as is well known in the art.

(Claim 5) Viewed from a second aspect, the present invention is directed to a method for reducing boron concentrations in and defective etching resulting therefrom of an insulating layer containing boron and phosphorus doped silicon oxide where the layer interfaces with a surfaces of a surface of a semiconductor wafer. The method comprises the steps of: seasoning a reaction chamber by flowing into it a mixture of gasses comprising silicon, boron, phosphorus, and ozone in predetermined proportions under set conditions of time, pressure, temperature and flow rates to deposit on inner walls and surfaces of the chamber a thin seasoning coating; placing a semiconductor wafer
in the chamber and depositing on it an insulating layer of boron-phosphorus-silicon-glass (BPSG) having a composition similar to the seasoning coating, and a thickness less than a micron, the average concentration of boron down through the BPSG layer being approximately constant, the BPSG layer covering devices formed in and/or on the semiconductor
wafer substantially without voids in preparation for the application of metalized conductors to the semiconductor wafer; and etching away selected portions of the BPSG insulating layer in preparation for the application of metalized conductors to the devices while leaving conductive surfaces of the semiconductor wafer remaining covered by the BPSG layer so as to avoid electrical short-circuits to the metalized conductors.

FIG. 1 shows a schematic cross-section of a portion of a semiconductor wafer in and on which two field effect transistors have been formed with an etched via which illustrates a problem which the present invention is directed to solving; and

Referring now to FIG. 1 there is shown a schematic illustration, in cross-section of a portion of a semiconductor wafer 10 having a substrate (body) 12 with a surface 12A. Field effect transistors 14 and 16 are formed in substrate 12 and on surface 12A. Transistor 14 comprises a drain region 18 and a source region 20 which are separated by a portion of substrate 12. Located on surface 12A is a gate dielectric layer 26 which is above and covers the portion of substrate 12a which separates drain region 18 from source region 20. A conductive gate layer 28 covers gate dielectric layer 26. Conductive Layer 28 can be doped polysilicon or metal. Transistor 16 is essentially identical to transistor 14 and comprises drain region 22, source region 24, a gate dielectric layer 30, and a conductive gate layer 32. Source region 20 of transistor 14 is separated from transistor 16 by a portion of substrate 12 and optionally by a dielectric region 25 (shown in dashed lines) formed in the portion of substrate 12 between transistors 14 and 16. Overlying transistors 14 and 16 and surface 12A is an insulating layer 34, which has a top surface 34A, through which has been etched a via 36 down to surface 12A.

The transistors 14 and 16, which may be transistors forming part of a high density DRAM, can be very closely spaced together. Horizontal spacing between
transistors 14 and 16 may be as small as a small fraction of a micron wide and the vertical depth from surface 34A to surface 12A can and typically is a number of times greater than this amount. This great depth-to-width ratio makes it difficult to fill the spaces between transistors 14 and 16 with insulation free of voids. Using only tetraethylorthosilicate (TEOS) in conventional fashion produces insulation which when annealed below 950.degree.
C. is not sufficiently "flowable" to always fill the deep narrow spaces between transistors 14 and 16 and other transistors (not shown) and devices (not shown) of the device 10. Accordingly, a mixture of TEOS with added amounts of triethylborate (TEB) and triethylphosphate (TEPO) is preferred to produce the insulating layer 34 since such insulation is sufficiently flowable when melted to fill the spaces between transistors 14 and 16 and other transistors and devices of wafer 10.

The insulating layer 34 is advantageously applied to the wafer 10, in one specific example, by flowing into a reaction chamber (not shown) at ambient temperature and a pressure of about 600 Torr (T) the following mixture of gasses: TEOS at 250 milligrams per minute (MGM), TEB at 112 mgm, TEPO at 50
mgm, and 4 liters per minute of helium mixed with 12.5% by weight of ozone. This flow of gasses into the chamber lasts for about 120 seconds. The pressure is then reduced to about 200T while increasing the flows of TEOS to 600 mgm, TEB to 160 mgm, and TEPO to 70 mgm, and with the same flow of helium and ozone,
for about another 80 seconds. The insulation deposited on the wafer 10 is

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fused into boron-phosphorus-silicon-glass (BPSG) by heating it to a suitably high temperature, as is well known. The insulating layer 34 thus deposited on the wafer 10 is void-free and has a thickness of about 0.6 micron in this specific example.

A conventional way of etching insulation such as the insulating layer 34, is to use buffered hydrofluoric acid (BHP) under conditions of temperature, time, concentration, etc., well known in the art. The insulating layer 34 is shown with a via (opening) 36 extending from a top surface 36A thereof down to surface 12A. Via 36 is typically formed by use of the etchant BHP. In via 36, boron concentration in the layer 34 near top surface 34A and down to close to surface 12A is not elevated and the walls of via 36 are essentially parallel until they reach close to surface 12A. However, because of boron-spikes in the insulating layer 34 near where it touches the surface 12A, the lower end of via 36 is etched away laterally (sideways), or undercut as indicated by brackets 24. This undercutting of layer 34 at 24 constitutes seriously defective etching of the via 36. The undercutting at 24 is shown extending to and laying bare small portions indicated of the gate layer 28 and the drain region 22 of transistor 16. The undercutting of insulation layer 34 at 24 is caused by too aggressive etching-away by the etchant BHP of insulating layer 34 where it has boron concentrations elevated above the average. When a metalized layer (not shown) is subsequently applied to fill the via 36 to provide an electrical conductor to the source of transistor 14, the metalized layer can contact the gate layer 28 of transistor 14 as well as the drain region 22 of transistor 16. This could electrically short the gate layer 28 and drain region 20 of transistor 14 to the source region 22 of transistor 16. This problem is avoided by the present invention which provides for "seasoning" or pre-conditioning of the processing chamber prior to applying the insulating layer 34 onto the wafer 10. "Seasoning" of the chamber inhibits the subsequent formation of boron-spikes in the insulation of a semiconductor device, as was previously explained. This in turn effectively prevents undercutting of subsequently formed insulation layer 34 at the lower ends of the via 36, as indicated by brackets 24. Using the inventive method results in the sides of the via 36 remaining substantially vertical down to the surface 12A. This leaves surfaces of the transistors 14 and 16 that are not to be contacted by metal deposited in via 36 still covered by portions of the insulating layer 34.

Referring now to FIG. 2, there is shown a graph 40 giving measured concentrations of the elements silicon (Si), boron (B), and phosphorus (P) in the insulation layer 34 of the wafer 10 (see FIG. 1). The graph 40 has a left-side vertical axis showing normalized values of concentrations of these elements in atoms per cc., a right-side vertical axis showing secondary ion intensity in counts/sec., and a horizontal axis showing depth in microns in the insulating layer 34 from its top surface 34A down to the surface 12A. This corresponds to the depth of a via 36 shown in FIG. 1. The graph 40 comprises a
first curve 42 showing concentration of silicon atoms as a function of depth into the insulation layer 34 of FIG. 1, a second curve 44 showing concentration of boron atoms as a function of depth into the insulation layer 34, and a third curve 46 showing concentration of phosphorus atoms as a function of depth into the insulation layer 34. The curves 42, 44, and 46 show measurements made by secondary ion mass spectroscopy (SIMS), a technique well known in the art.

2. The method of claim 1 wherein the insulating layer on the device is fused into boron-phosphorus-silicon-glass (BPSG) such that voids and empty spaces in
the insulation are avoided.

5. A method for reducing boron concentrations in an insulating layer comprising the steps of: seasoning a reaction chamber by flowing into it a mixture of gasses comprising silicon, boron, phosphorus, and ozone in predetermined proportions under set conditions of time, pressure, temperature and flow rates to deposit on inner walls and surfaces of the chamber a thin seasoning coating; placing a semiconductor wafer in the chamber and depositing
on it an insulating layer of boron-phosphorus-silicon-glass (BPSG) of a thickness less than a micron, the average concentration of boron down through the BPSG layer being approximately constant, the BPSG layer covering devices formed in and/or on the semiconductor wafer substantially without voids in preparation for the application of metalized conductors to the semiconductor wafer; and etching away selected portions of the BPSG insulating layer in preparation for the application of metalized conductors to the devices while leaving conductive surfaces of the semiconductor wafer remaining covered by the
BPSG layer so as to avoid electrical short-circuits to the metalized conductors.

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